

# CHEMICAL VAPOR DEPOSITION OF TITANIUM

## Related Applications

5 This application is a continuation-in-part of U.S. Application Serial  
No. 09/030,705, filed February 25, 1998, which is hereby incorporated by reference in  
its entirety.

## Field of the Invention

10 The present invention relates to a method for manufacturing semiconductor  
devices, and more particularly, to a method for depositing titanium layers on a substrate.

## Background of the Invention

15 Device density in integrated circuits (ICs) is constantly being increased. To  
enable the increase in density, device dimensions are being reduced. As the dimensions  
of device contacts get smaller, device contact resistance increases, and device  
performance is adversely affected. Methods for decreasing device contact resistance in  
ICs are needed to obtain enhanced device and IC performance.

20 Device contacts with reduced resistance may be created by forming certain  
metals on a silicon semiconductor base layer. These metals react with the underlying  
silicon, for example, to form silicides. Silicide device contacts are desirable because  
they reduce the native oxide on silicon. The native oxide is undesirable because it  
increases the contact resistance.

25 In one embodiment, titanium is used to form silicide device contacts for two  
reasons. First, titanium silicide has superior gettering qualities. Also, titanium silicide  
forms low resistance contacts on both polysilicon and single-crystal silicon.

Titanium silicide device contacts are normally formed with the following  
process. First, a thin layer of titanium is formed on top of the silicon base layer, such as  
a substrate. The titanium adjoins active regions exposed by contact holes in an isolating  
layer, such as an oxide, above the silicon base layer. Then, the silicon base layer is

annealed. As a result, the titanium reacts with the active regions of silicon to form titanium silicide.

However, because titanium cannot be readily deposited in a pure form, additional processing steps are required to form titanium silicide device contacts.

5 Titanium precursors, such as titanium tetrachloride, are commonly available and can be used to form titanium. Titanium tetrachloride, though, can only be reduced at temperatures exceeding 1000 degrees Celsius with certain reducing agents. At these temperatures, the silicon base layer will be damaged. Therefore, there is a need for a method of forming titanium from titanium precursors at lower temperatures.

10 Furthermore, the resistance of device contacts can be adversely increased by conductive layers coupled between the device contacts and other components. The conductive layers may be formed by the same metal layer used to form the device contacts. As device dimensions shrink, the contact holes become relatively deeper and narrower. Also, the walls of the contact holes become steeper, and closer to vertical.  
15 As a result, most metal deposition techniques form conductive layers having relatively small step coverage, and hence relatively high resistance. Step coverage is the ratio of the minimum thickness of a film as it crosses a step, to the nominal thickness of the film on flat regions, where thickness is generally measured perpendicular to the surfaces of the step and flat regions, and where the resultant value is usually expressed as a  
20 percentage. Thus, the effective contact resistance is increased at lower values of step coverage. Therefore, there is also a need for a method of forming conductive layers having increased step coverage to reduce effective device contact resistance.

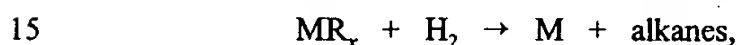
Conformal layers of titanium having good step coverage have been previously formed at lower temperatures with chemical vapor deposition. Such techniques are  
25 disclosed in U.S. patents 5,173,327, 5,273,783 and 5,278,100, which are hereby incorporated by reference. However, alternative, effective and efficient techniques for forming titanium films are desired.

### Summary of the Invention

The present invention provides a method, and a corresponding resulting structure, for forming conformal titanium films supported on a substrate of an integrated circuit (IC) by forming a seed layer supported by the substrate, and then reducing a titanium precursor with the seed layer. In one embodiment, the seed layer comprises a main group element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony. The seed layer is formed by combining a first precursor and a reducing agent by chemical vapor deposition (CVD). Then, titanium is formed by combining a second precursor with the seed layer by CVD.

In another embodiment, the present invention may further comprise the step of annealing the titanium to form titanium silicide.

In another embodiment, forming the seed layer further comprises forming a seed layer according to the following chemical process (I):



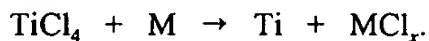
wherein: M is a main group element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony;

R is an alkyl group; and

20  $x$  is some integer value determined by the valence of M.

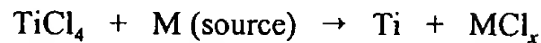
In one embodiment, chemical process (I) is performed at a temperature between approximately 100 and 600 degrees Celsius.

In yet another embodiment, the step of forming titanium further comprises the step of combining the seed layer with the second precursor that is titanium tetrachloride according to the following chemical process (II):



In one embodiment, chemical process (II) is performed at a temperature between approximately 100 and 600 degrees Celsius.

In yet another embodiment, titanium may be formed in a single step according to the following chemical process (III):



In one embodiment, chemical process (III) is performed at a temperature between approximately 100 and 700 degrees Celsius.

In yet a further embodiment, the present invention may be an IC comprising a layer of a titanium alloy, coupled to a titanium silicide contact. In yet another embodiment, the present invention may be a memory comprising a memory array operatively coupled to a control circuit and an I/O circuit. The memory array, control circuit and I/O circuit comprise a layer of a titanium alloy coupled to titanium silicide contacts. In yet another embodiment, the titanium alloy may comprise titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony. In still another embodiment, the titanium alloy may comprise titanium and zinc.

It is a benefit of the present invention that high step coverage metal layers can be formed. Further features and advantages of the present invention, as well as the structure and operations of various embodiments of the present invention, are described in detail below with reference to the accompanying drawings.

#### Brief Description of the Figures

Figure 1A is a cross-sectional view of a contact hole that has been etched through an insulative layer to an underlying semiconductor substrate.

Figure 1B is a cross-sectional view of the contact hole of Figure 1A, comprising titanium and titanium silicide film.

Figure 2 is a cross-sectional view of the contact hole of Figure 1A, comprising a film of second reducing agent.

Figure 3A is a cross-sectional view of the contact hole of Figure 1A, comprising a titanium film.

Figure 3B is a block diagram of a memory.

### Detailed Description of the Invention

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable persons skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention. The terms wafer and substrate used in the following description include any semiconductor-based structure having an exposed surface with which to form the integrated circuit structure of the invention. Wafer and substrate are used interchangeably to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

The subsequently described methods will be in the context of using zinc as a metal seed layer. However, other seed layers are suitable for use with the various embodiments of the invention, as will be described.

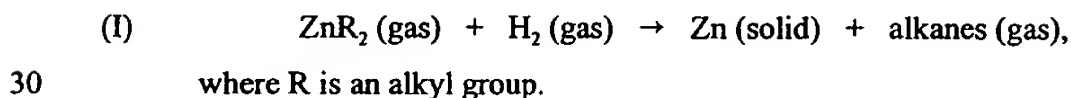
In order to manufacture a device contact in an integrated circuit 19, a contact hole 10, as shown in Figure 1A, is etched through an insulating layer 12, such as borophosphosilicate glass (BPSG) or silicon dioxide ( $\text{SiO}_2$ ). As a result, an active region 17 of underlying semiconductor base layer or substrate 14, is exposed. A device contact is then formed on the exposed active region 17 in the following manner.

Chemical vapor deposition (CVD) is used to form a conformal layer of titanium or titanium alloy on the integrated circuit 19 by a subsequently described method. CVD is further described in U.S. Patent No. 5,278,100. In one embodiment, the conformal layer has a step coverage of at least one hundred percent in the contact hole 10, even for a high aspect ratio contact hole (i.e., a contact hole that is much deeper than it is wide).

As a result, a low resistance layer of titanium or titanium alloy 16 is formed on the insulating layer 12, as shown in Figure 1B. A portion of the layer 16 is formed as a low resistance device contact 18 of titanium silicide over the active region 17.

In another embodiment, a cold wall-hot substrate reactor is used to form the conformal layer of titanium or titanium alloy. In one embodiment, a cold wall-hot substrate reactor is used for blanket depositions as this design is efficient in regard to precursor consumption. In one embodiment, first, a conformal film of a seed layer 22 comprising zinc is deposited on the insulator 12 and substrate 14, as shown in Figure 2. The seed layer 22 is formed with CVD by combining a first reducing agent 24 with a first precursor 26, which are injected into the CVD reactor which is represented in block form at 29. In another embodiment, the seed layer 22 that is zinc may be formed by combining a first precursor 26 that is a dialkyl zinc or trimethyl zinc compound with a reducing agent 24 that is hydrogen.

When performing this step, the integrated circuit 19 is mounted on a substrate holder in the CVD reactor 29. The substrate 14 is heated to a temperature within a range of approximately 100 to 600 degrees Celsius and at a pressure approximately between 1 millitorr and 1 atmosphere. Alternatively, the temperature may range from approximately 300 to 550 degrees Celsius, or approximately 350 to 450 degrees Celsius. In one embodiment, the temperature is approximately 400 degrees Celsius. Also, alternatively, the pressure may range from approximately 10 millitorr to 100 torr. In one embodiment, the pressure is approximately 1 torr. A carrier gas of helium, argon or nitrogen may be used at a flow rate of between approximately 1 and 200 sccm. Alternatively, the flow rate may range between approximately 20 sccm and 1 liter. In one embodiment, the pressure is approximately 200 sccm. The first precursor 26 and the reducing agent 24 contact the heated silicon base layer and insulating layer 12, and form the seed layer 22 on the integrated circuit 19. This chemical process (I) is exemplified below:

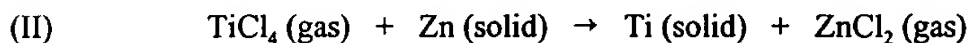


First reaction products 28, such as gaseous alkanes, resulting from the formation of the seed layer 22 exit from the CVD reactor 29 through an exhaust manifold. The thickness of the seed layer 22 formed on the integrated circuit 19 is between approximately 5 and 50 angstroms. However, the present invention envisions forming a seed layer 22 that is thicker.

Next, the seed layer 22 is converted to a layer 16 of titanium or a titanium alloy. As illustrated in Figure 3A, a titanium precursor 32, such as titanium tetrachloride, is combined with the seed layer 22 by CVD to form a conformal layer 16 of titanium or titanium alloy in lieu of the seed layer 22.

When performing this step, the integrated circuit 19 is mounted and heated in the CVD reactor 29 to a temperature within a range of approximately 100 to 600 degrees Celsius and at a pressure approximately between 1 millitorr and 1 atmosphere.

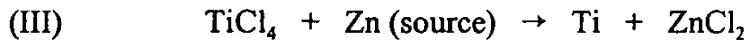
Alternatively, the temperature may range from approximately 100 to 700 degrees Celsius, approximately 300 to 550 degrees Celsius, or approximately 350 to 450 degrees Celsius. In one embodiment, the temperature is approximately 400 degrees Celsius. Also, alternatively, the pressure may range from approximately 10 millitorr to 100 torr. In one embodiment, the pressure is approximately 1 torr. A carrier gas of helium, argon or nitrogen may be used at a flow of between approximately 1 and 200 sccm. Alternatively, the flow rate may range between approximately 20 sccm and 1 liter. In one embodiment, the pressure is approximately 200 sccm. When the titanium precursor 32 contacts the seed layer 22 on the integrated circuit 19, the compounds form a conformal layer 16 of titanium or a titanium alloy. The chemical process (II) is exemplified below:



Second reaction products 34 resulting from the formation of the titanium or titanium alloy exit from the CVD reactor 29 through the exhaust manifold. Part or all of the seed layer 22 is converted to a layer 16 of titanium or titanium alloy. If this process step is conducted for a sufficient period of time, all of the seed layer 22 will be

converted to a layer 16 of titanium. However, if not all of the seed layer 22 is converted to a layer 16 of titanium, a layer 16 of titanium alloy, including the seed layer 22, will be formed on the integrated circuit 19. These steps may be repeated to form thicker layers.

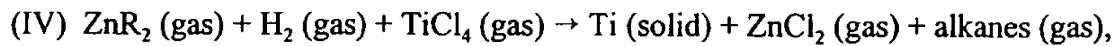
- 5           In another embodiment, the layer 16 of titanium or titanium alloy can be formed during a single CVD step, as exemplified by chemical process (III) below:



- 10   The zinc can be provided from one of many types of sources, including gaseous and solid sources. In one embodiment of such a single CVD step, the seed and titanium layers 22, 16 can be formed substantially simultaneously. The titanium or titanium alloy layer 16 can be formed by combining a first precursor 26, such as a dialkyl or trimethyl zinc compound, with a reducing agent 24, such as hydrogen, and a titanium precursor 32, such as titanium tetrachloride. When performing the CVD step, the integrated circuit 19 is mounted and heated in the CVD reactor 29 to a temperature within a range of approximately 100 to 600 degrees Celsius at a pressure of approximately between 1 millitorr and 1 atmosphere. Alternatively, the temperature may range from approximately 100 to 700 degrees Celsius, approximately 300 to 550  
15   degrees Celsius, or approximately 350 to 450 degrees Celsius. In one embodiment, the temperature is approximately 400 degrees Celsius. Also, alternatively, the pressure may range from approximately 10 millitorr to 100 torr. In one embodiment, the pressure is approximately 1 torr. A carrier gas of helium, argon or nitrogen may be used at a flow rate of between approximately 1 and 200 sccm. Alternatively, the flow rate may range  
20   between approximately 20 sccm and 1 liter. In one embodiment, the pressure is approximately 200 sccm. When the first precursor 26 and the reducing agent 24 contact the heated silicon base layer and insulating layer 12, they form the seed layer 22 on the integrated circuit 19. Then, when the titanium precursor 32 contacts the seed layer 22, a conformal layer 16 of titanium or titanium alloy is formed on the integrated circuit. The  
25   resulting layer 16 of titanium or titanium alloy has a thickness between approximately 5  
30



and 50 angstroms. However, the present invention envisions forming a thicker layer 16 titanium or titanium alloy. The chemical process (IV) is exemplified below:



5 where R is an alkyl group.

The reaction products 28, 34 exit from the CVD reactor 29 through the exhaust manifold.

Subsequently, the integrated circuit 19 is annealed at a temperature of between  
10 approximately 250 to 750 degrees Celsius. Alternatively, the temperature may range from approximately 250 to 800 degrees Celsius. In one embodiment, the temperature is approximately 700 degrees Celsius. As a result, the titanium in the layer 16 of titanium or titanium alloy proximate to the silicon is converted to titanium silicide ( $\text{TiSi}$ ,  $\text{TiSi}_2$ ,  $\text{Ti}_3\text{Si}_5$ , or combinations thereof) to form the low resistance device contact 18. For via  
15 level applications, the anneal is not required. The via comprises a tungsten or aluminum fill on top of the layer 16 which is formed on top of a conductor (also represented by reference number 17) with an optional TiN layer therebetween.

In yet another embodiment, the low resistance device contact 18 of titanium silicide may be formed over the active region 17 when the layer 16 of titanium or  
20 titanium alloy is formed by CVD on the integrated circuit 19 at a temperature of between approximately 250 to 750 degrees Celsius. Alternatively, the temperature may range from approximately 250 to 800 degrees Celsius. In one embodiment, the temperature is approximately 700 degrees Celsius. Upon device contact 18 formation, additional metal layers, such as titanium nitride and tungsten, may be subsequently  
25 formed over the device contact 18 and layer 16 of titanium or titanium alloy.

In another embodiment, the integrated circuit 19 is a memory 300 in Figure 3B, such as a dynamic random access memory. The memory 300 may include an array of memory cells 302, control circuit 304, I/O circuit, word line decoder 308, digit, or bit, line decoder 310, and sense amplifier 312 coupled in a manner known to one skilled in

the art. Each of the aforementioned elements of the memory 300 includes contacts 18 and layers 16 of titanium, or titanium alloy, formed in the manner described above.

As noted above, other seed layers are suitable for use with the various embodiments of the invention. In one embodiment, the first precursor 26 is an alkane of the form  $MR_x$ , where M is an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; R is an alkyl group; and  $x$  is some integer value determined by the valence of M. The value of  $x$  is generally equal to a valence of M, e.g., when M has a valence of 3 as does aluminum,  $x$  equals 3. M may be capable of having more than one valence. Such alkane precursors may be used to form the seed layer 22. Chemical process (I) for the formation of seed layer 22 may then be written in its more general form:

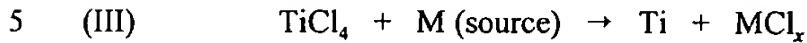
(I)  $MR_x \text{ (gas)} + H_2 \text{ (gas)} \rightarrow M \text{ (solid)} + \text{alkanes (gas)},$   
15 wherein: M is an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony;  
R is an alkyl group; and  
 $x$  is some integer value equal to the valence of M.

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In similar fashion, chemical process (II) for the formation of the layer 16 of titanium or titanium alloy may be written more generally as:

(II)  $TiCl_4 \text{ (gas)} + M \text{ (solid)} \rightarrow Ti \text{ (solid)} + MCl_x \text{ (gas)}$   
25 wherein: M is an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and  
 $x$  is some integer value equal to the valence of M.

In another embodiment, where the formation of the layer 16 of titanium or titanium alloy is performed in a single step, chemical process (III) may be written more generally as:

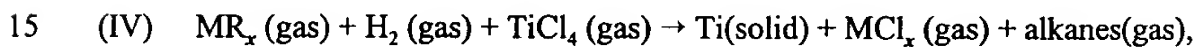


wherein: M is an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

x is some integer value equal to the valence of M.

10

In a further embodiment, where the formation of the layer 16 of titanium or titanium alloy is performed in a single CVD step, chemical process (IV) may be written more generally as:



wherein: M is an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony;

R is an alkyl group; and

20 x is some integer value equal to the valence of M.

The various embodiments of the present invention provide high step coverage, low resistivity titanium silicide device contacts to silicon, or titanium contacts to metal at the via level, formed at a relatively low temperature. Use of the various alkane precursors permits formation of a titanium layer without depletion of an underlying silicon or other base layer.

It is to be understood that the above description is intended to be illustrative, and not restrictive. Many other embodiments will be apparent to those of skill in the art upon reviewing the above description. For example, other titanium precursors, such as tetradimethyl amino titanium (TDMAT) can be used to form layers 16 and device

21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100																				
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100